Optimizing Real-Time Systems

(OVSTR)

DigiCosme Research Days
April 12\textsuperscript{th}, 2016
Outline

- Presentation of the OVSTR working group
- Subject and outcomes of first meeting
- Next meetings and outlook
What is OVSTR?

Subject: optimization of real time systems
- Currently performed at a single level of design only
- Instead focus on cross-layer optimizations:
  From high-level models down to the hardware level
- Keywords: real-time task scheduling, WCET analysis, probabilistic analysis, high-level modeling, compilers, (predictable) computer architecture, multi-core, network-on-chips, applications

Goal: identify scientific problems for collaboration
- Foster discussion at the end of meetings (reserve 1 hour per meeting)
- Community involved to find next meeting topics

Website: https://digicosme.lri.fr/gt+ovstr
OVSTR Meetings

One-day meetings focusing on a specific subject

- 2-3 meetings per year
- Open to everyone interested

Morning Session:

- Invited talks focusing on the state-of-the-art
- Complementary topics
- Coordinated presentations

Afternoon Session:

- Presentations focusing on a given contribution
- Proposed by community
First OVSTR meeting (October 15, 2015)

- Subject: cache issues in WCET analysis and scheduling of real-time tasks
- 33 participants (France, Germany, Luxembourg)

Morning sessions (invited):

- Jan Reneike (Saarland University, Germany):
  « Bounding the Cache-Related Preemption Delays »
- Pascal Richard (University of Poitiers):
  « Hard Real-Time Scheduling with Cache-Related Preemptions delays »

Afternoon session:

- 4 talks (LTCI/Telecom ParisTech, Inria, University of Brest, University of Luxembourg)

3 talks of outstanding/best papers of RTNS 2015

- Slides of all task available on website
Cache Issues

Slides extracted from invited talks ... (thanks to them!)

Why use preemptive scheduling?

- Preemption often increases schedulability of task sets.
- Tasks with short deadlines are often unschedulable non-preemptively.

Example

Given: Two periodic tasks $T_1$ and $T_2$, with periods $P_1 = 2$, $P_2 = 8$, deadlines $D_1 = P_1$, $D_2 = P_2$, and execution times $C_1 = 1$, $C_2 = 3$. 

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Jan Rainke
Cache-Related Preemption Delay
October 15, 2015
Outcome

Synthesis of the discussions

- Should scheduler be aware of more information coming directly from the application level?

- Should the notion of tasks be refined, e.g., by in execution phases having possibly different properties?
  - Capture more semantics from higher levels of design
  - Extend current task models or even redefine them

Submission of an ANR proposal: SWORTS

- Enhance real-time system design flow:
  
  Optimize timing properties based on high-level models (CPAL), covering code generation, WCET analysis, and task scheduling.
Next meeting

May 23rd at LTCI/Telecom ParisTech

- Subject: parallelization of real-time tasks
- Registration available here: [https://digicosme.lri.fr/gt+ovstr](https://digicosme.lri.fr/gt+ovstr)
  - Afternoon: slots for shorter talks are still available!

Morning session:

- Laurent George (ESIEE):
  « Real-time multiprocessor scheduling of parallel tasks »
- Christine Rochange (University of Toulouse):
  « Timing analysis of parallel tasks running on parallel architectures »

List of potential upcoming subjects:

- Network-on-chips (traversal times and task mapping), design of time-predictable hardware platforms, reproducibility, code generation