Opportunities and challenges of many cores for future avionics applications

A journey starting from low criticality

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SUMMARY

− 01 – Kalray MPPA® Architecture
− 02 – Safran Electronics & Defense expectations
− 03 – FADEC – HM functions
− 04 – PoC Architecture demonstrator
− 05 – Conclusions & perspectives
01 – MPPA® Architecture

A Clustered Manycore Processor Architecture for Embedded and Accelerated Applications
Compute cluster (x16)
- 16 cores + 1 RM
- 2MB SRAM (aggreg.)

IO Cluster (x2)
- 8 cores
- 4MB SRAM

Interfaces (x2)
- PCIe gen3
- 4x Ethernet 10Gbps (aggreg. 40Gbps)
- Interlaken interfaces (NoCX)
- 64 GPIO (DNA)
- SPI, I²C, UART
Network on Chip
- Interconnect each cluster (compute or IO)

Torus 2D interconnect

Route control

DMA-NoC
- RDMA
**IO cluster role**
- IO processing → Compute Cluster specialized into computing only (no IO)

**RM of compute cluster role**
- Allocate jobs to cores,
- Initiate communications with other clusters
02 – SAFRAN Expectations

About MPPA® into airborne systems
SAFRAN EXPECTATIONS FOR EXPERIMENTATION

- Computing performance vs power consumption
  - The GFLOPS versus power consumption tradeoff is important in airborne systems

- Evolution capabilities
  - Support future highly demanding applications for performance / Watt

- Temporal partitioning control
  - Computable WCET / WCRT for critical applications

- Multi-applications integration
  - Heterogeneous DALs on the same chip
  - Different security levels e.g. for Information Systems connected to Open networks
03 – EASA Expectations
MPPA® into airborne systems
Objective: Crashes are unacceptable

- All parts should be designed fully functional in all situations
- Not feasible
- Trade-off (feasibility/risk): level of reliability
- FMEA: failure mode & impact analysis

Mean: How to ensure reliability/performance

- By quality of the development process (e.g. correct by construction)
- By design: system has to be **deterministic & safe**
- Met **objectives** using **activities** (see next slide)

Certification: How to prove the reliability & safety demonstrations?

- Show that the **process** was correctly applied (quality review; activities checklist)
- Show that the designer **fully master the system behavior** (engineer review)
AERONAUTICAL CERTIFICATION 2/4

➔ Example of HW activities required for certification
  ▪ Plans documents (PHAC, …), and summary of activities (HAS, …)
  ▪ Specifications, verifications
  ▪ Identification of P/N of processors
  ▪ Datasheet, errata, manufacturer data analysis, …

➔ Example of SW activities (some identical to HW)
  ▪ Component tests
  ▪ WCET demonstration
  ▪ Control coupling / data coupling, …

➔ Multicore (MCP) usage raised new concerns for authorities:

EASA

Federal Aviation Administration

CRI-MCP

CAST-32
→ **Interferences & resources allocations**

Interference occurs whenever a resource is shared between cores (NoC, DDR, …)

→ Core resource usage interferes the use of this resource by other core
  - Increase latency (access conflicts), dead-locks
  - Loss of bandwidth (loss of data)

→ Require complete control of:
  - **resources capabilities** (HW activity).
  - **path** between core and resources (ex. NoC with latency or possible data loss)
  - **resources usage** (bandwidth, latency, nb access, …) by each core (SW activity).
Software activities

- Control coupling / Data coupling (between cores) software running in parallel shall be mastered
- WCET demonstration execution time shall be mastered (interferences/latencies !)
- Verification environment require all software running (all representatives interferences are present) except for specific system (IMA: robust partitioning)
- Dynamic software (SMP, reconf, …) not advised (too many paths to verify)

Conclusion

- System approach is important (domain usage, …)
- SW has to fully assimilate the complexity of HW
04 – PoC demonstrator

Experiment integration of multiple applications on a single massively parallel processor
DEMONSTRATOR (PROOF OF CONCEPT)

1,000,000 Float32 / 8s + Control

20ms cycle

Andey 400MHz
APPLICATIONS MAPPING

Motor simulator (SIMMOT)

Motor control (GUIMMOT)

Motor state (EICAS)

Host x86 (Linux)

Input data generation code + retrieval of results (HM)

ECU (1 core)

IO FADEC

I/O Cluster

I/O HM

IO Eth

ETH

DPH

MPPA256

PCI0

DDR

PCI0

DDR
MULTI-CLUSTER SPEED-UP FACTORS

- **Limitations**
  - Communication costs dominate computations
  - Inter frame dependencies limit maximum parallelism
CONTROL OF SHARED RESOURCES

➔ Shared resources will cause interference in SW execution!
  ▪ Have to be controlled / mitigated (c.f. EASA CRI-MCP)

➔ SW architecture have to be selected to limit shared resources, HW is ready to limit resources sharing (RM, IO clusters, …)

  ▪ Inter-cluster shared resources
    ▪ Symmetric design of the I/O: 2 independent groups
    ▪ NoC: routing capabilities, simplified design

  ▪ Intra-cluster shared resources
    ▪ Independent memory busses on SRAM
    ▪ No cache coherency mechanism

  ▪ Into core
    ▪ Simple design
05 – Conclusions & perspectives
CONCLUSIONS

DAL A-C applications

- Still at a very experimental stage, only mono-core mode in a cluster is considered safe for *time critical functions*
  - Into the demonstrator, the light FADEC code *fits on one core*.
  - Determinism of the access path to the I/O and the NoC partitionning capabilities. To be studied

- **Enforced partitioning capabilities** with proper NoC routers’ configuration
  - Security and interferences control to be deeply evaluated

DAL D-E applications

- For *non-time critical functions*, it is possible to use **all cluster cores**.
  - To study: measure the interference level into the NoC

- High potential of possible optimization of the algorithms (and of the demonstrator SW architecture)

- High speed-up factor but:
  - I/O bandwith is the limitation not computation
  - Requires to re-design the algorithms
Given CRI MCP

- Still long journey to reach DAL A/B and C levels but MPPA architecture is promising
- Non time-critical applications are therefore quite relevant also in avionics
- Benchmarks in the CAPACITES project

High potential for demanding health monitoring applications

- Scalability issues to be addressed
- Joint work with Safran Aircraft Engines (ex-Snecma) still on-going in the ASSUME project