WCET Analysis in Shared Resources Real-Time Systems with TDMA Buses

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in collaboration with:
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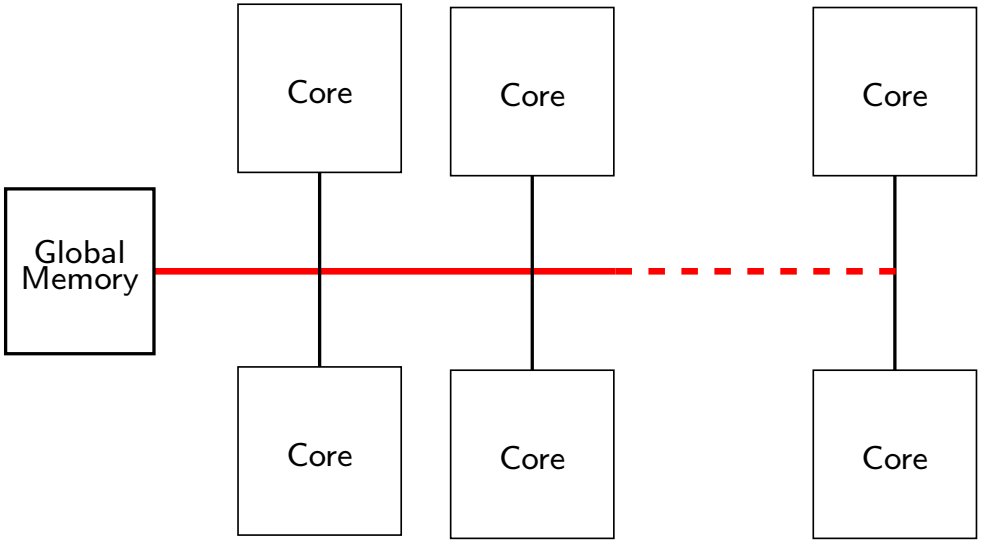
Precise static WCET analysis: combining path and TDMA analyses

Main idea

- TDMA causes no direct interference
- Task execution time does not depend on what is executed on other cores
- New analysis that combines:
  - a precise analysis on when memory accesses happen (path analysis)
  - a precise analysis on tdma slot (bus analysis)
- Use of SMT encoding

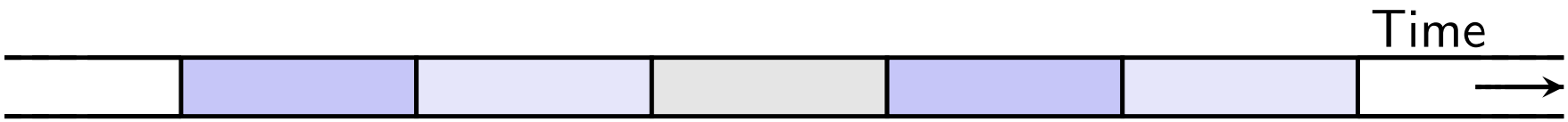
Outline

TDMA bus for Multicore



- Shared resources: contention, access delays
- Time Division Multiple Access (TDMA) arbitration policy
  - Time triggered policy
  - Assign fixed time slots to each core

Time Division Multiple Access



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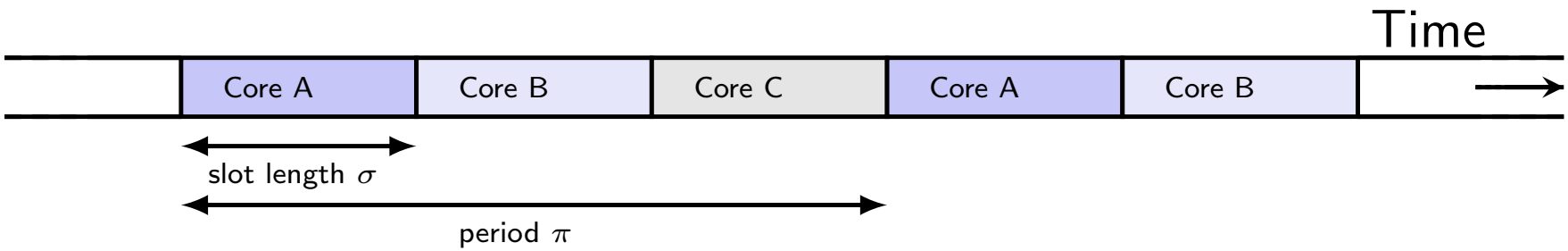
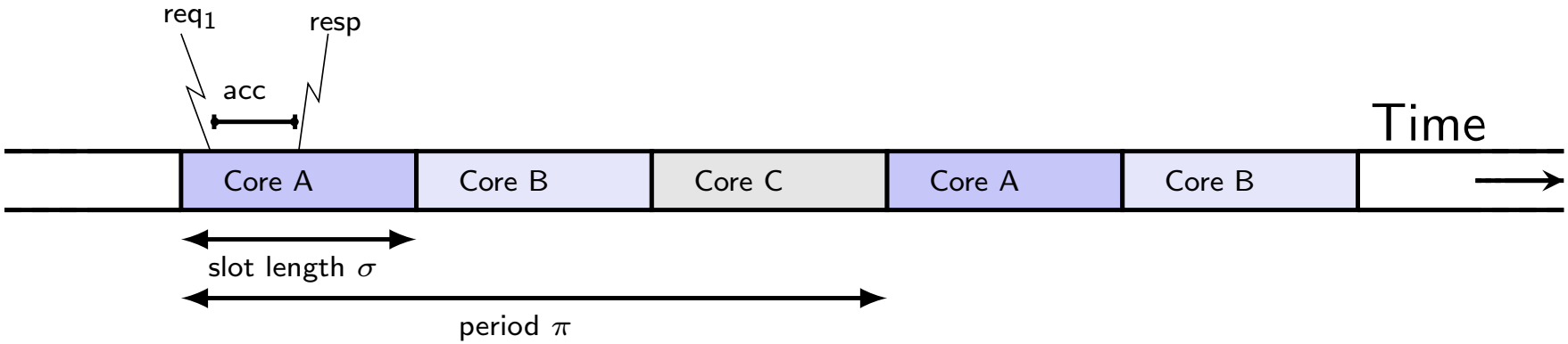


Time Division Multiple Access

Core A viewpoint:



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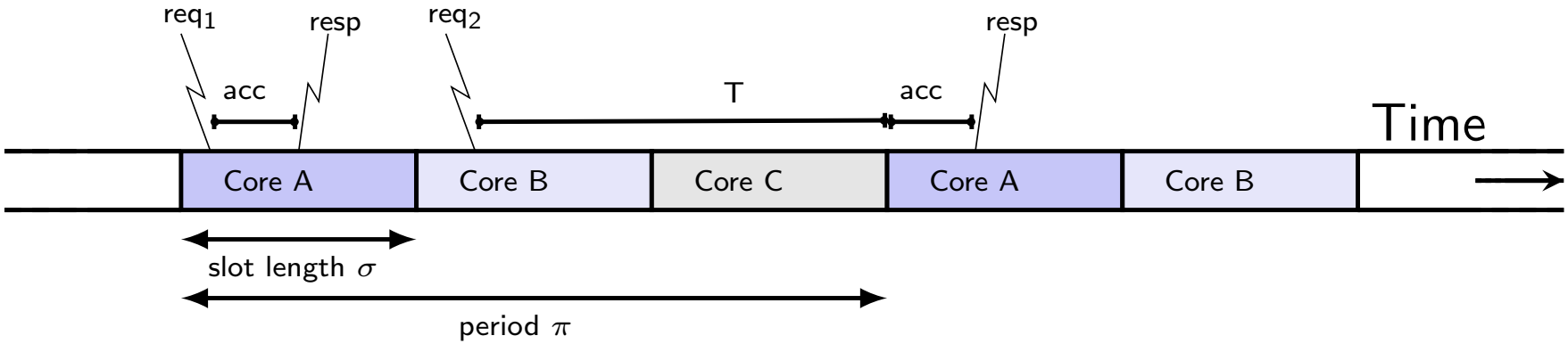

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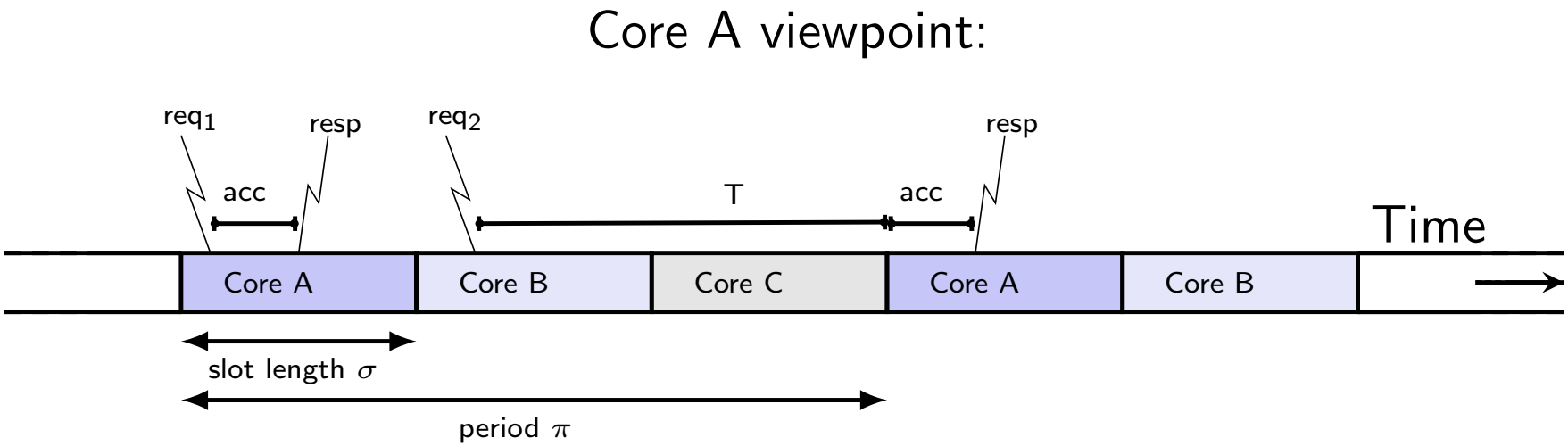

- *acc* execution time of a granted request
- T waiting time to grant requests $\in [0, \pi - (\sigma - acc)[$

  Pessimistic approach: *Worst-Case(T)* $= \pi$ - (σ - *acc*)

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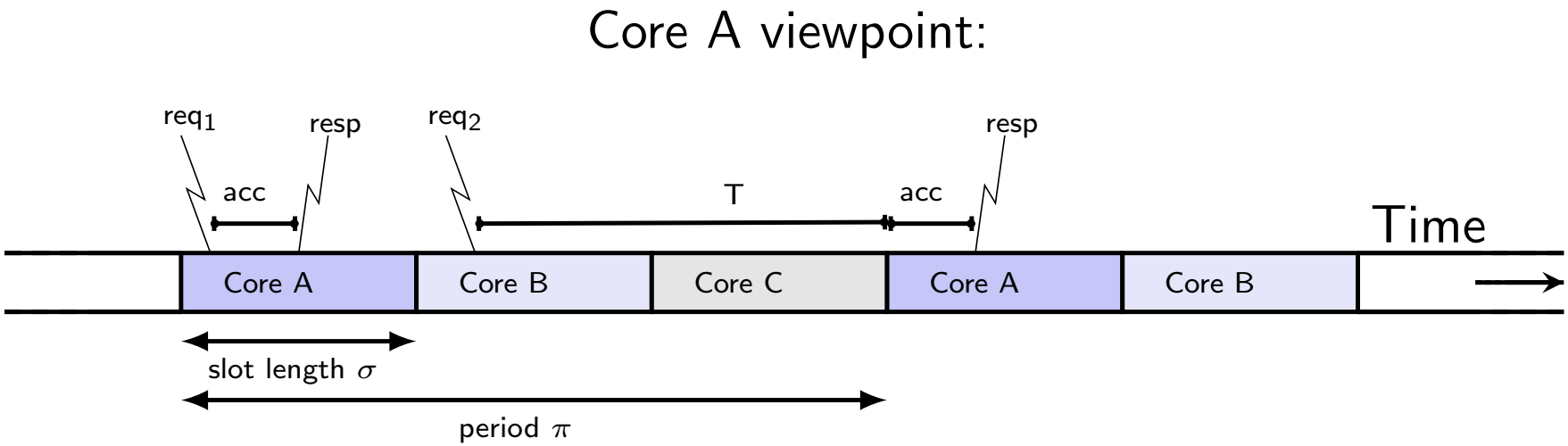

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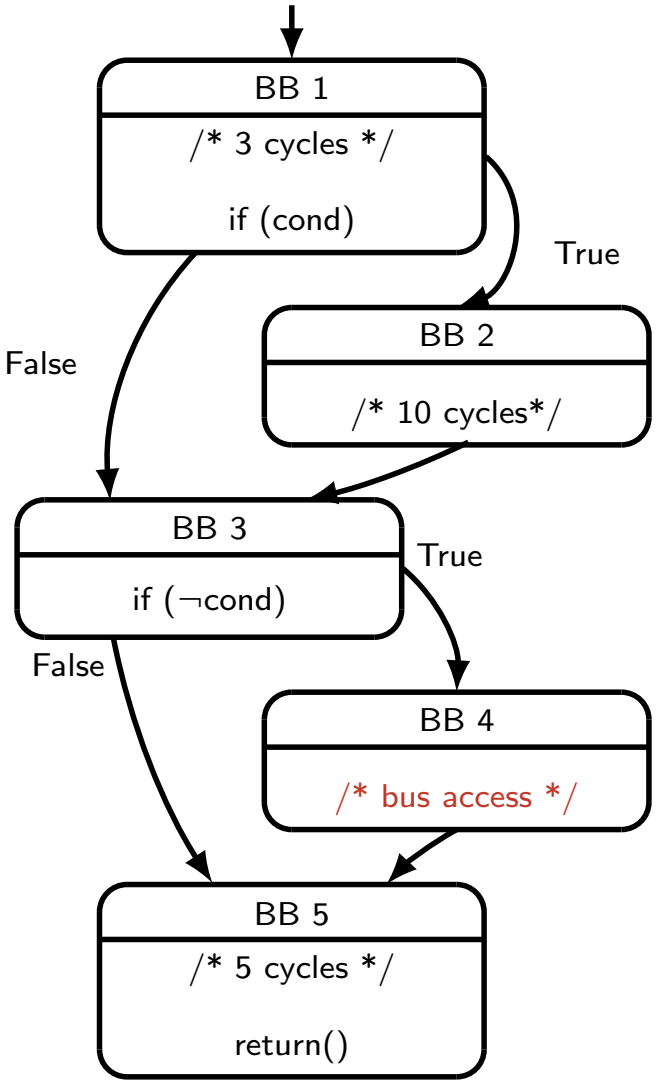
  Pessimistic approach: $Worst\text{-}Case(T) = \pi$ - $(\sigma$ - $acc)$
- Offset relative to the TDMA period:

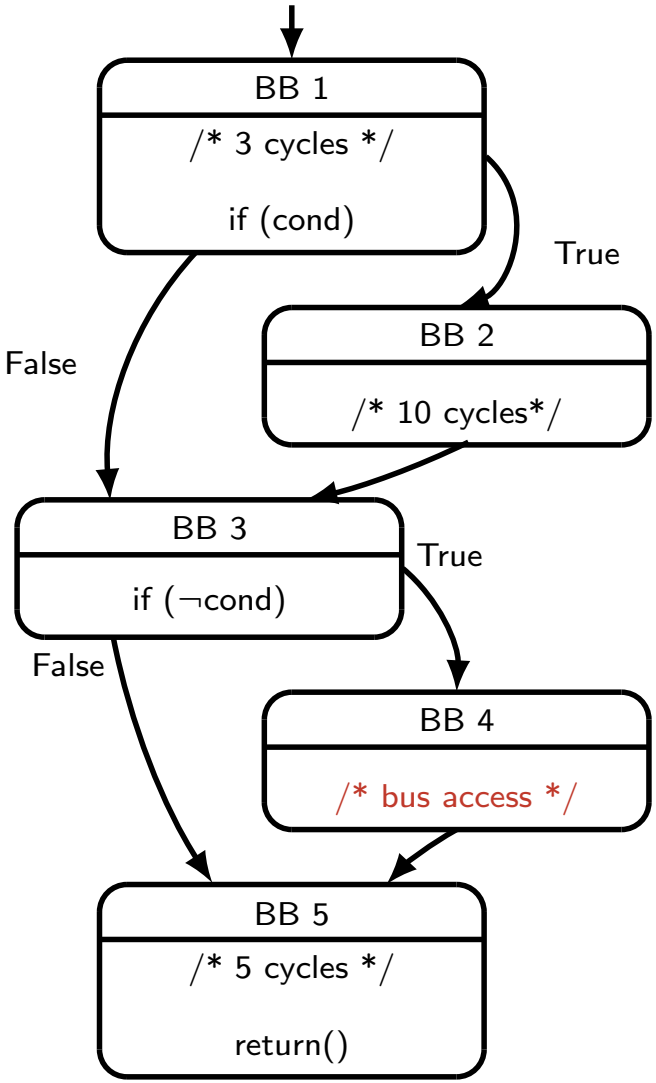
$$Offset(req) = time\_instant(req) \mod \pi$$

Motivation: WCET Analysis of TDMA



Goal: Estimate the WCET

Motivation: WCET Analysis of TDMA

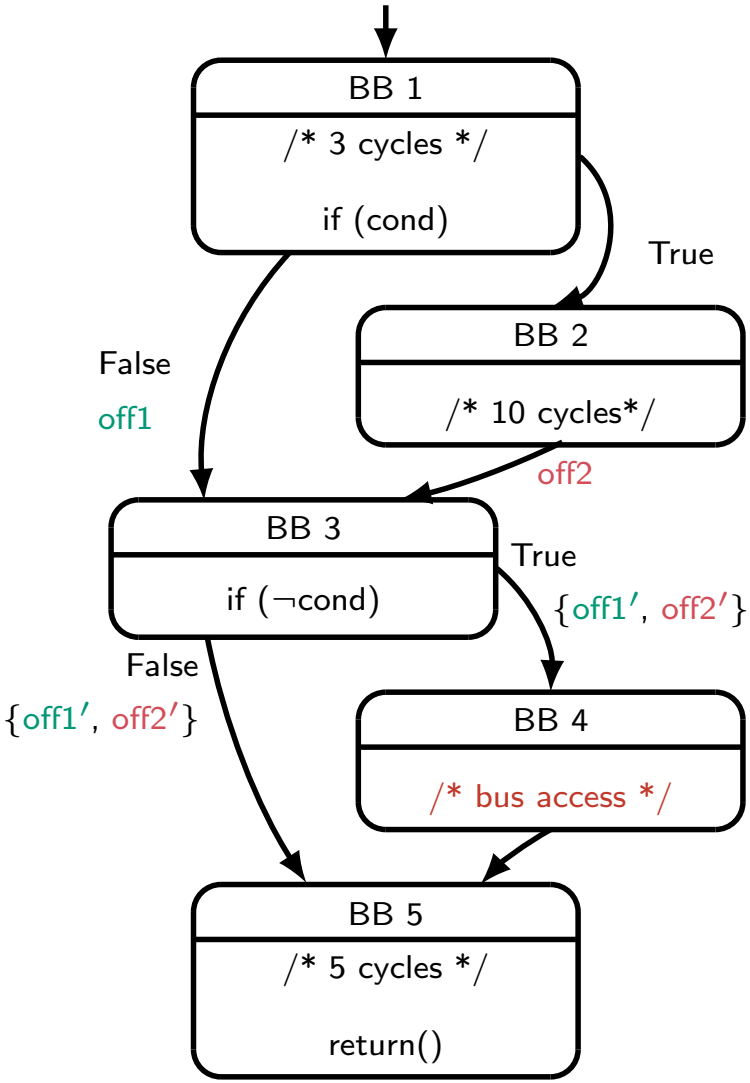


cost$=\pi - \sigma + 2\ acc$

Goal: Estimate the WCET

- Option 1: Worst-case everywhere.

Motivation: WCET Analysis of TDMA



Goal: Estimate the WCET

- Option 1: Worst-case everywhere.
- Option 2: Capture all possible offsets

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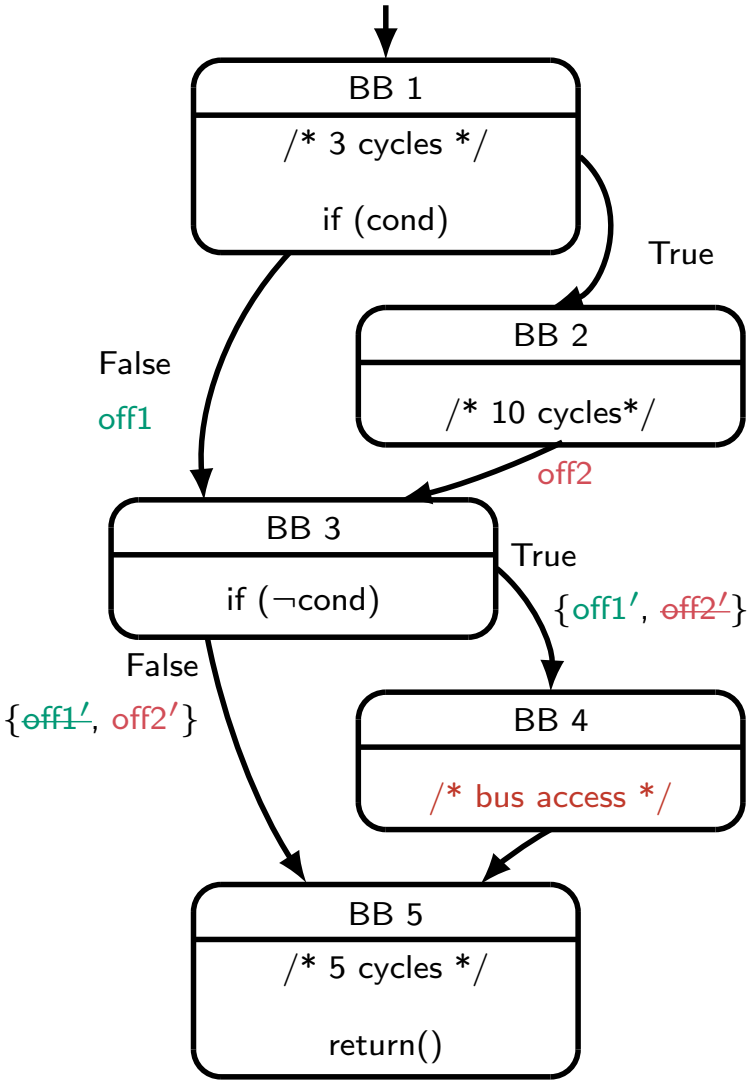

Goal: Estimate the WCET

- Option 1: Worst-case everywhere.
- Option 2: Capture all possible offsets
- Option 3: Feasible Path Analysis

Contribution

TDMA Bus Analysis

Kelter et al., RTS'14

Chattopadhyay et al., SCOPES'10

Feasible Path Analysis with SMT

Henry et al. LCTES'14

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Contribution:

Compute WCET by encoding the semantics and shared resource accesses into an optimization problem (SMT)

WCET Analysis by SMT Encoding

- Bounded Model Checking
  - Encode the semantics into a Satisfiability Modulo Theory problem

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$$\underbrace{\text{SMT query}}_{\text{assert}(\bigwedge \text{expr})} = \text{“Is there a trace with correct semantics ?”}$$

- SMT-solver response:
  - SAT: There is a feasible execution path
  - UNSAT: There is no feasible execution path

WCET Analysis by SMT Encoding

- Bounded Model Checking
  - Encode the semantics into a Satisfiability Modulo Theory problem
- Add execution times on the paths

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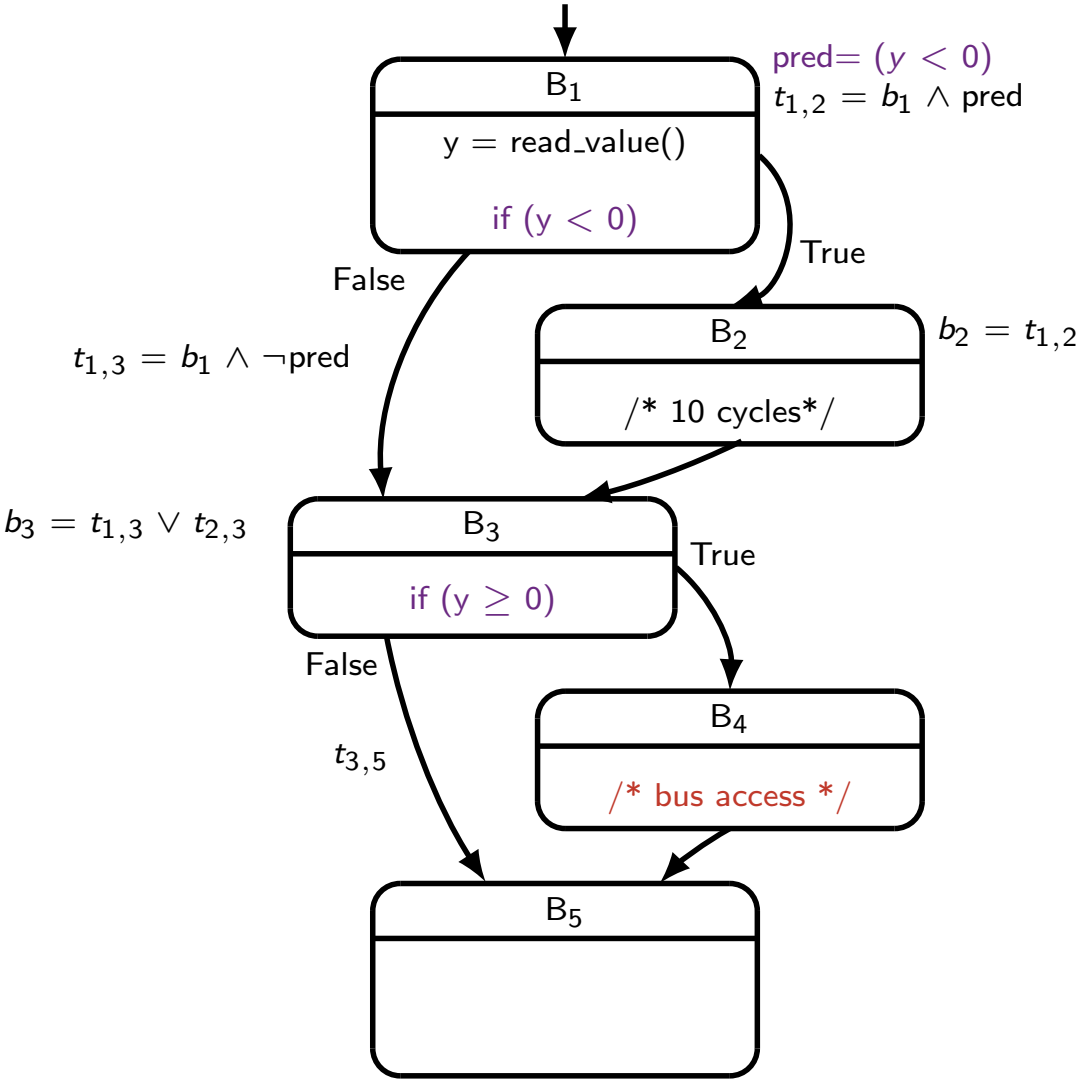
Goal:

Find the smallest X, such that Execution Time $> X$ is UNSAT

Example: Semantics and Timing Encoding



- b_i "*true*" if B_i executed
- $t_{i,j}$ "*true*" if *transition* $B_i \rightarrow B_j$ taken

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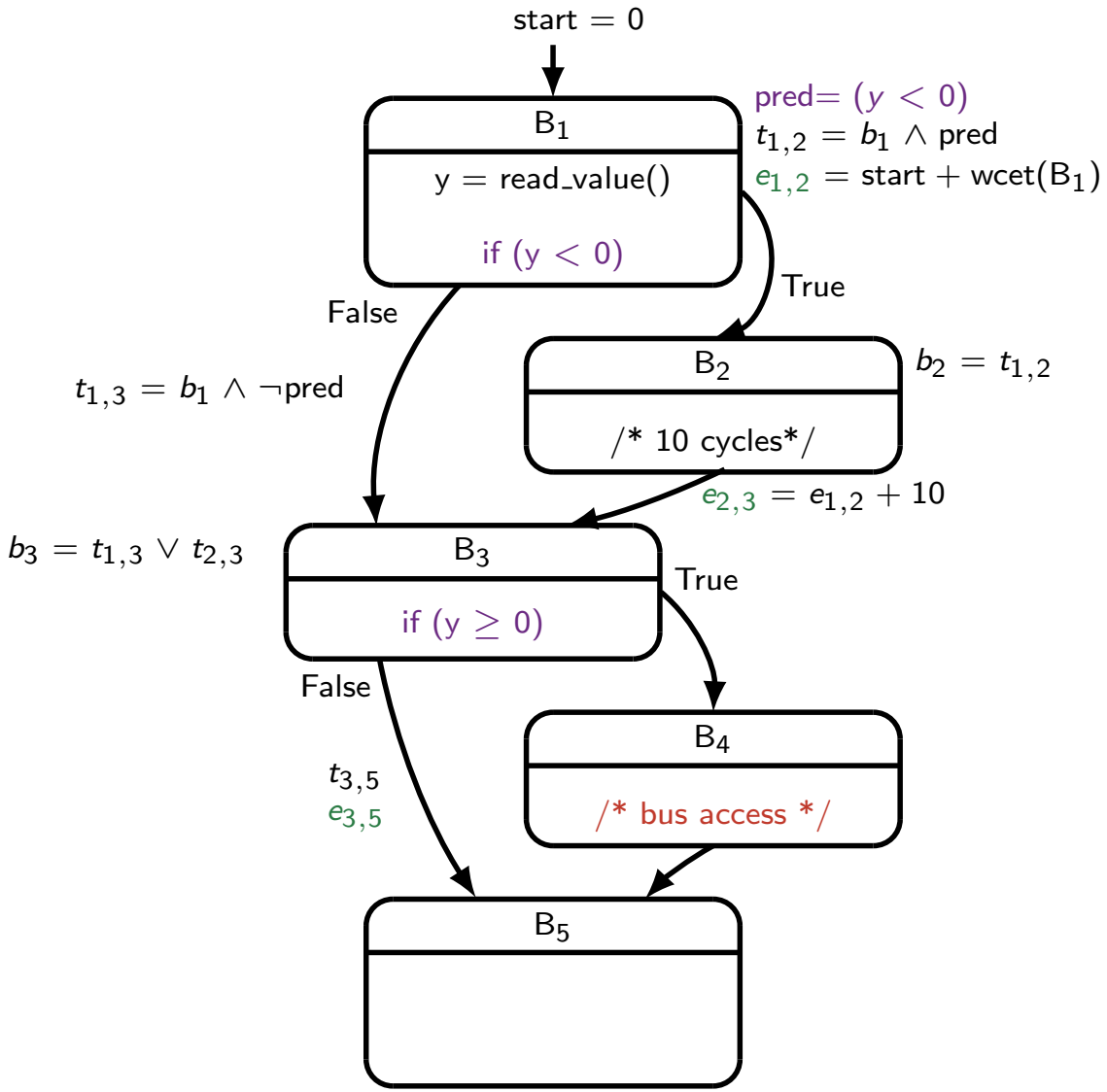

execution time = if $t_{3,5}$ then $e_{3,5}$ else $e_{4,5}$

- b_i "*true*" if B_i executed
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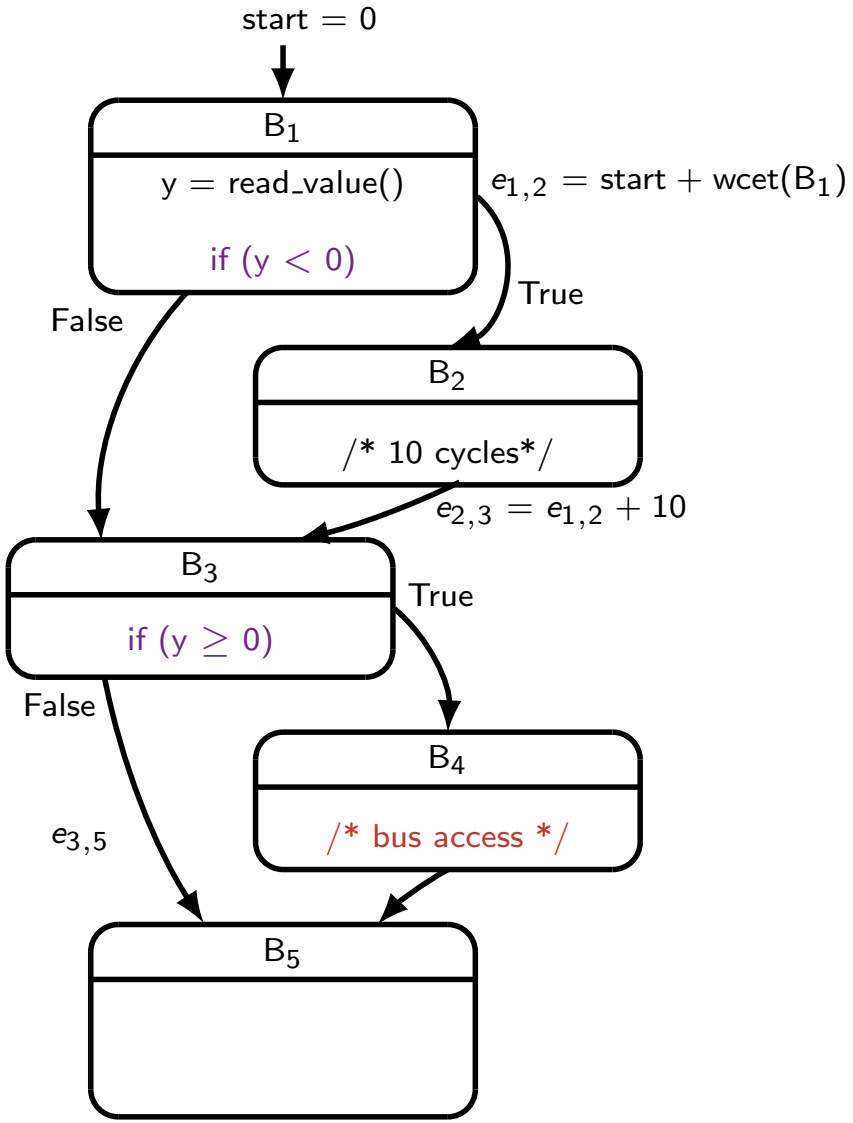

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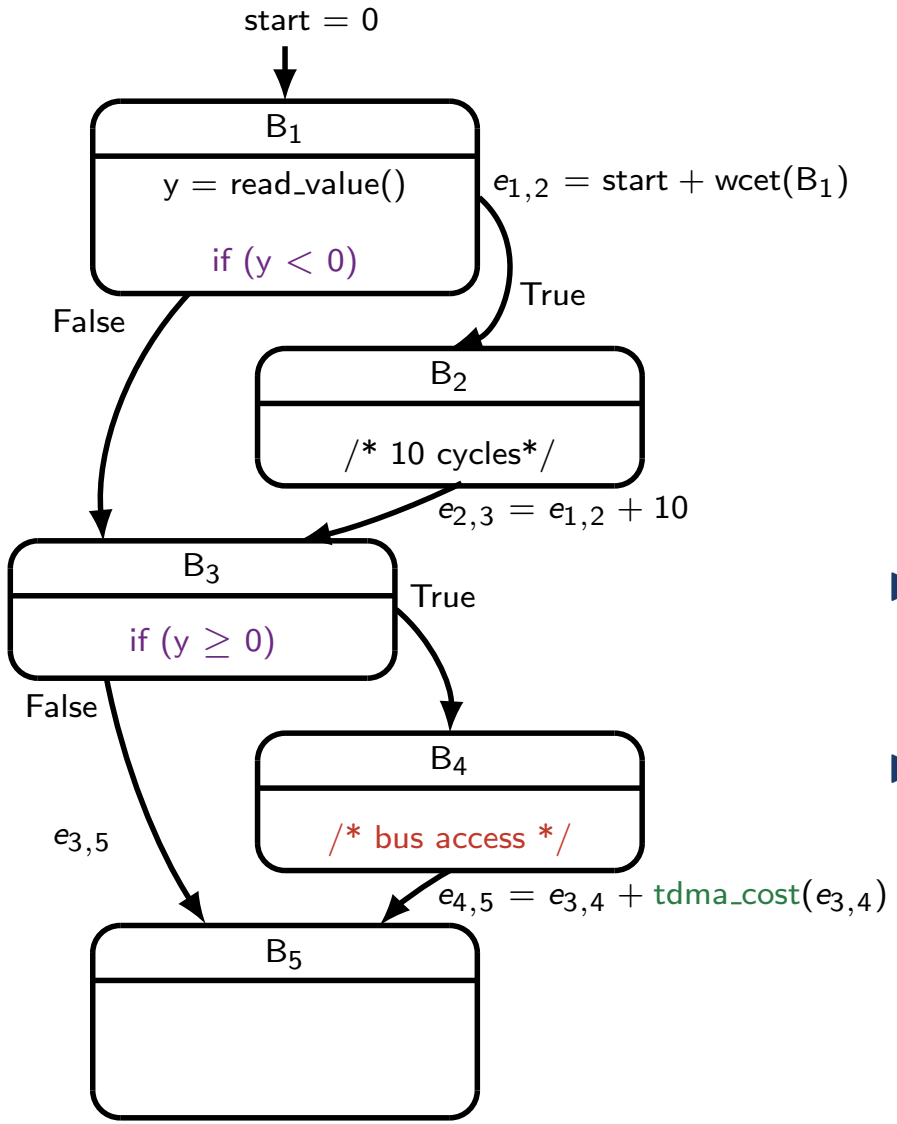
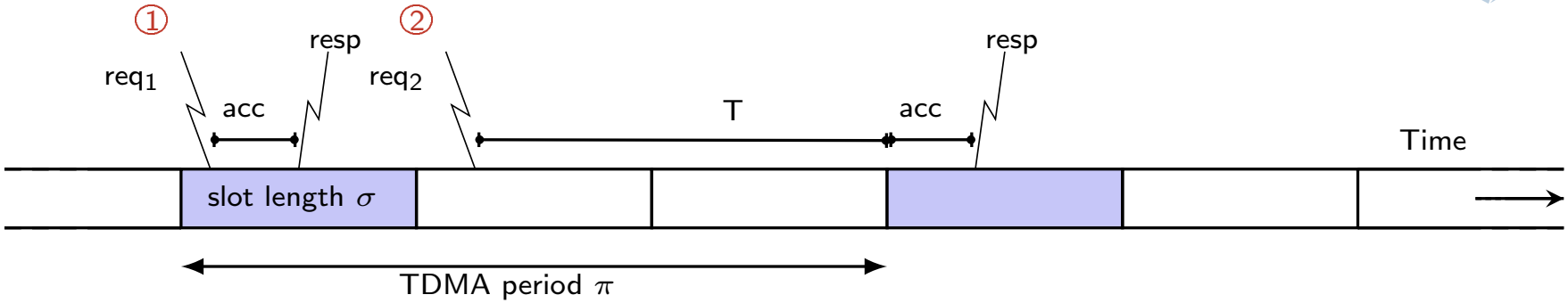


execution time = if $t_{3,5}$ then $e_{3,5}$ else $e_{4,5}$

- $e_{i,j}$ *execution time* at transition $B_i \rightarrow B_j$
- tdma_cost() execution time of a bus access

TDMA delay: SMT Encoding

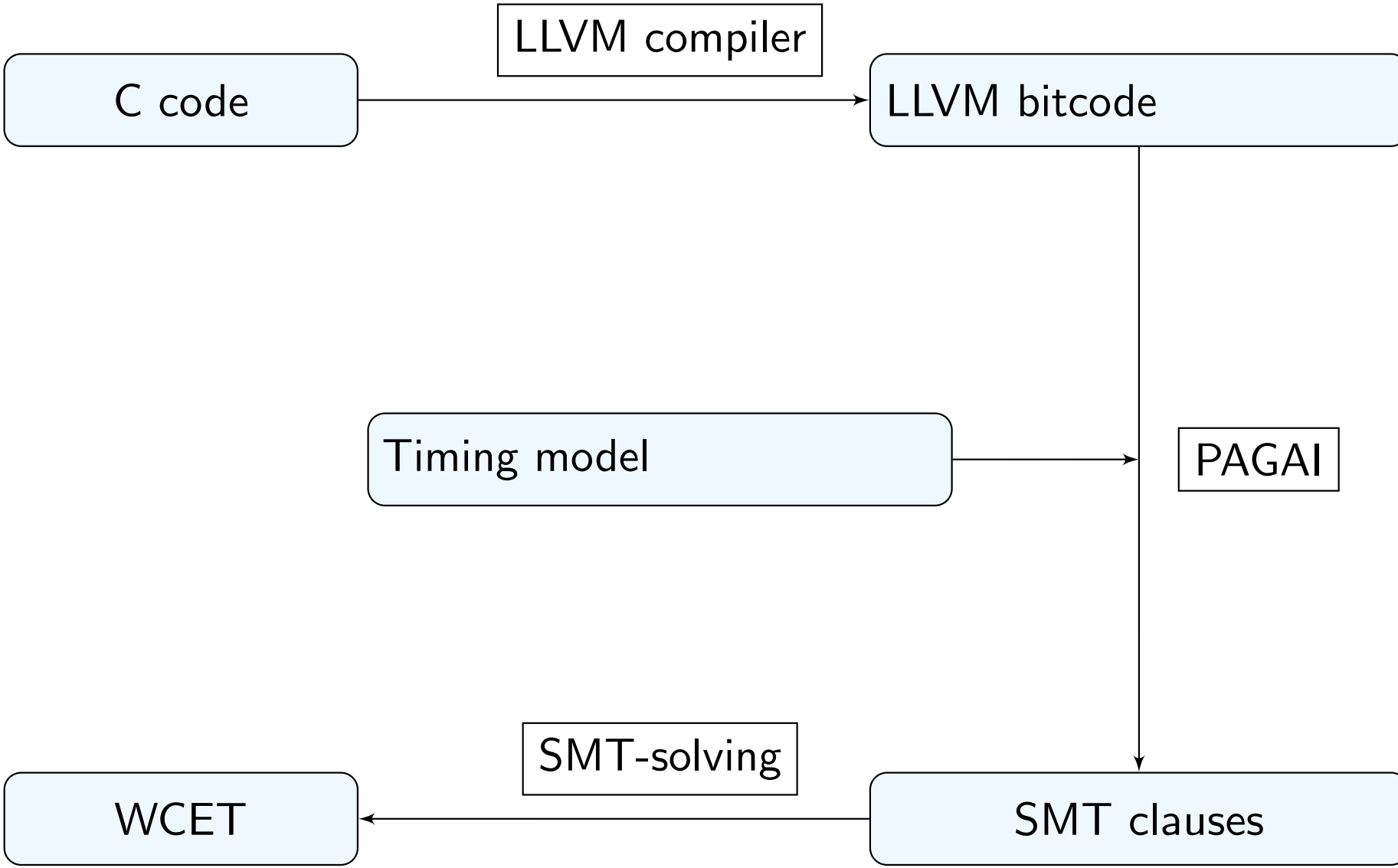


Algorithm *tdma_cost*: returns the execution time of a bus access

Require: e_{entry}

1: $\text{offset}_{entry} \leftarrow e_{entry} \mod \pi$
2: **if** $\text{offset}_{entry} \in [0, \sigma - acc[$ **then** /* offset is inside the slot */①
3: **return** *acc*
4: **else** /* offset is outside the slot */ ②
5: **return** $(\pi - \text{offset}_{entry}) + acc$
6: **end if**

Proof-of-Concept Implementation



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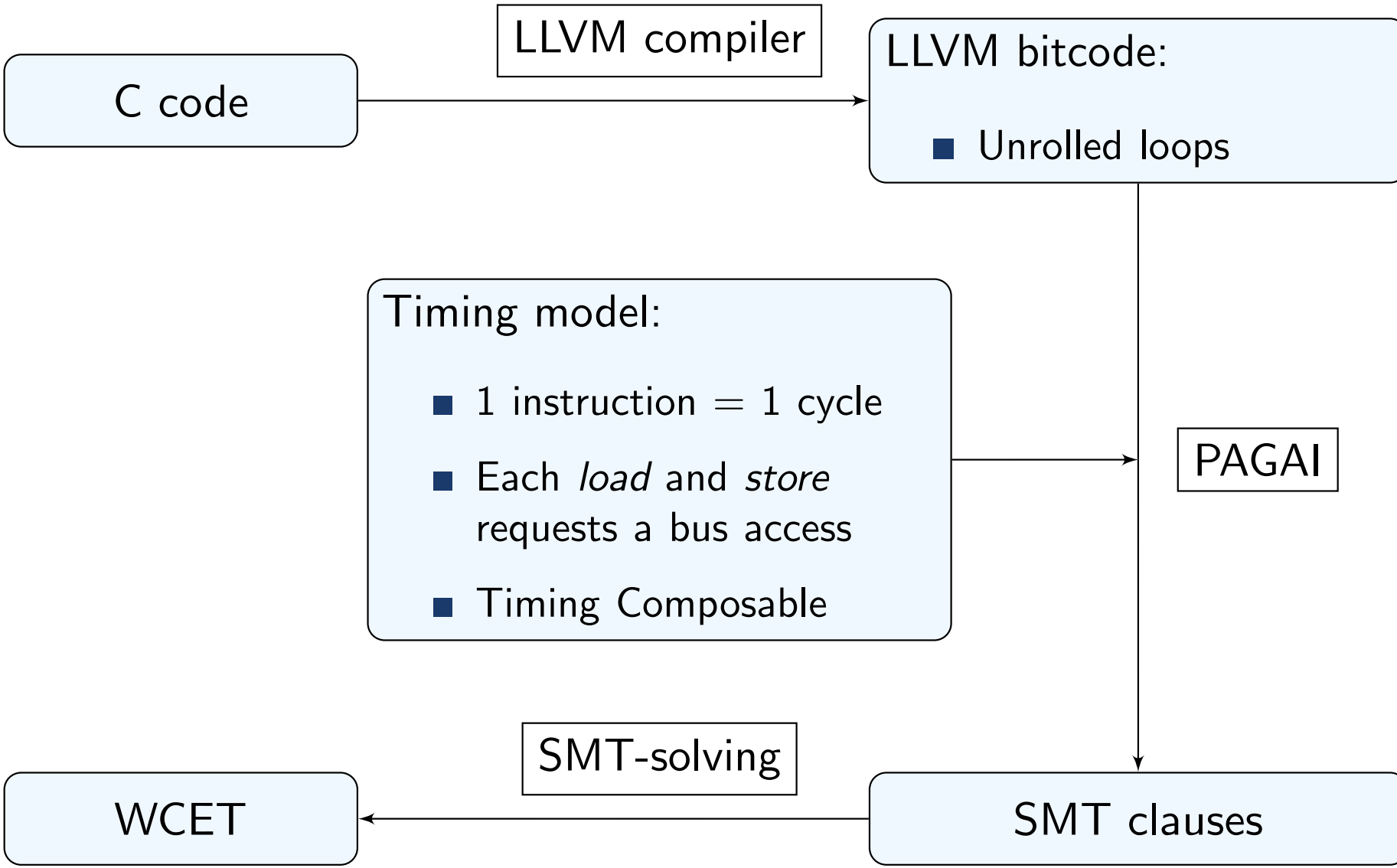
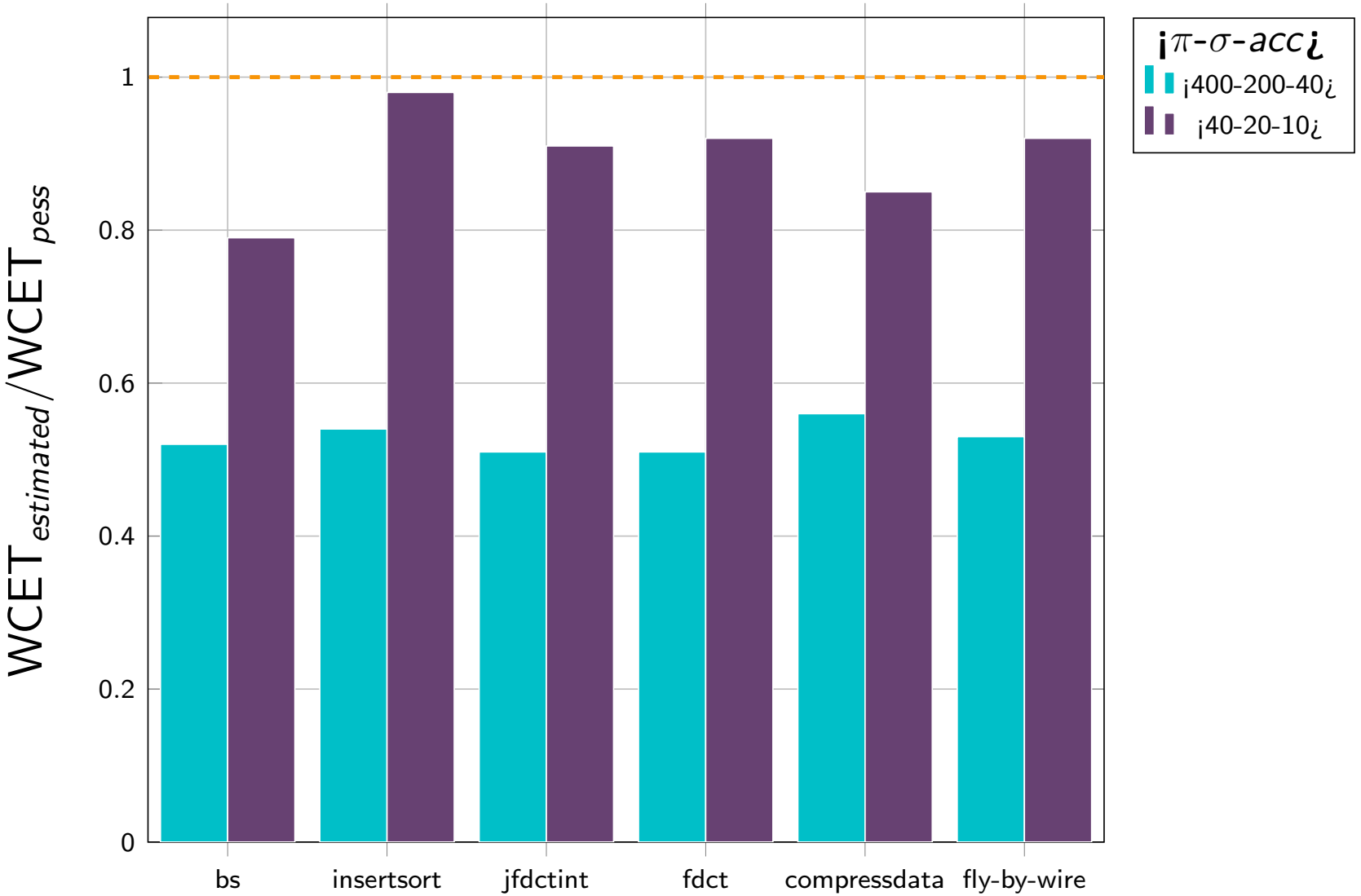


Evaluation

Name	Description	#LLVM instr.	#bus access
bs	Binary search	231	12
insertsort	Insertion sort on a reversed array	493	65
jfdctint	Discrete Cosine Transformation	2334	448
fdct	Fast Discrete Cosine Transform	2502	385
compressdata	Data compression program adopted from SPEC95	674	131
fly-by-wire	UAV fly-by-wire software	2815	515

Table: Benchmark description

Evaluation



Estimated WCET of the benchmarks with different configurations of the TDMA bus

Evaluation

	$< \pi, \sigma, acc >$	
Name	$< 40, 20, 10 >$	$< 400, 100, 40 >$
bs	**0.45s**	0.98s
insertsort	1.37s	6.56s
jfdctint	44.10s	48.54s
fdct	41.36s	34.57s
compressdata	4.66s	3.23s
fly-by-wire	28.78s	**149.01s**

Analysis time

Summary

- SMT encodings for TDMA access
- Validation with small but relevant benchmarks

Why does it work?

- Feasible Path Analysis combined with the WCET computation
- Best-case of gain: All requests are within the TDMA slots
- Worst-case of gain: All requests have worst-case delay

Discussion

- Very good approach for TDMA
- No TT: analysis depends on other tasks = this kind of approach does not scale anymore
- Missing step: implementation on binary level

References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